A GaAs Power Amplifier for 3.3 V CDMA/AMPS Dual-Mode Cellular Phones

Sung-Jae Maeng, Soung-Soon Chun, Jong-Lam Lee, Chang-Seok Lee, Kwang-Jun Youn, and Hyung-Moo Park, *Member, IEEE*

***Abstract*—For CDMA/AMPS dual-mode cellular phones, a power amplifier operating at 3.3 V has been developed for the first time. It consists of linear GaAs power MESFET's and an output matching circuit which reduces the second and the third harmonics. The amplifier shows an output power of 31.5 dBm and a power-added efficiency of 61% for AMPS mode. The third-order intermodulation distortion and the fifth-order one are measured to be −32 dBc and −45 dBc at an output power of 26 dBm for CDMA mode.**

I. Introduction

A MOBILE COMMUNICATION system changes from the analog system to the digital one as subscribers increase. CDMA cellular phone system using offset QPSK modulation signal will be serviced in Korea from 1996. The power amplifier of a CDMA cellular phone requires both high power-added efficiency (PAE) and good linearity. Nonlinearity creates intermodulation distortion (IMD) and raises the bit error rate (BER), which is the key issue to be solved in digital communication systems. The nonlinearity is mainly determined by the third order intermodulation distortion (IM3). The conventional approach for achieving linear power amplification with low distortion is to use class A power amplifiers, or to back off 3 dB from the 1 dB compression point, which reduces the PAE. Therefore, output power should be high enough to achieve sufficient output power in the linear region.

In CDMA transmitter applications of power amplifier, the IMD must be balanced with PAE in the linear region of output power. The effective radiated output power and the IMD at the maximum output power of the amplifier should be 23 dBm and less than −30 dBc, respectively, for the CDMA mobile station, considering a typical loss of 3 dB between the power amplifier and the antenna. Therefore, a power amplifier should have an output power of 26 dBm with both IMD less than −30 dBc and PAE more than 30%. Meanwhile, the output power and PAE are required to be 31 dBm and 55%, respectively, for the AMPS transmitter applications, considering the same power loss as for the CDMA case. There are several reports on the techniques to compensate for nonlinearity of MESFET's such as Cartesian feedback [1], [2], nonlinear single tone simulation [3], load-pull measurements by the two-tone test [4]. However, the linearizing circuits are not suitable for low-cost and small-size power amplifiers, and the design by nonlinear simulation needs an accurate nonlinear model of high power MESFET. These difficulties can be overcome by developing a linear power MESFET for both CDMA and AMPS applications.

The supply voltage of the cellular phone has been decreased to 3.3 V in order to reduce the volume and weight of the phone. Several power amplifiers with a low supply voltage have been reported [5]–[7]. The performance of the reported power amplifiers has an output power of 31.1 dBm with PAE of 60% at 3.5 V for analog phones [5], and PAE of 49% at an output power of 31.1 dBm with a supply voltage of 3.6 V for digital phones [7]. However, there was no report on a power amplifier for dual-mode cellular phones, until now.

In this work, we have developed a power amplifier operated at a supply voltage as low as 3.3 V for the CDMA/AMPS dual-mode cellular phone, which simultaneously satisfied the linearity for CDMA mode and the output power and PAE for AMPS mode. For the circuit design, the optimum load and source impedances of the MESFET were determined by the tradeoff between the power performance and the linearity using the load-pull method. The output matching circuit was designed to have low impedances for the 2nd and the 3rd harmonic frequencies in order to reduce the harmonics.

II. MESFET Design and Fabrication

In order to obtain the linearity for CDMA together with the output power and PAE for AMPS mode in the 3.3 V operation power amplifier, it is important to develop highly efficient and linear power MESFET's with a supply voltage of 3.3 V. There are several sources causing intermodulation such as transfer characteristics and output impedance matching of the MESFET. Most of the distortion arises from the nonlinear dependence of the drain current on gate bias. A constant transconductance with gate bias at a drain voltage can be obtained by a vertically stepped doping profile in the channel of the MESFET rather than a uniform doping profile [8].

Fig. 1 shows a low-high doped channel structure which was used in the fabricating power MESFET's to obtain the constant transconductance [9]–[11]. The structure consists of a 1 μm thick undoped buffer layer, a thin active layer doped with mid $10^{17}/cm^3$ (high-doped layer), a thick active layer

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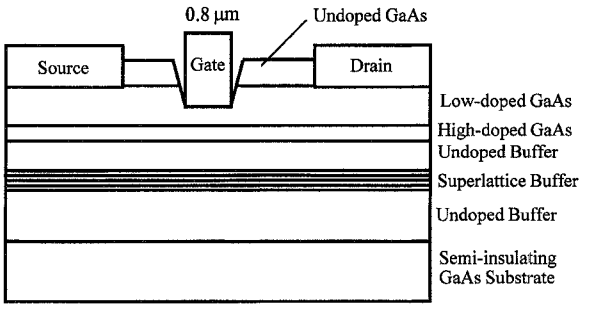


Fig. 1. Structure of a low-high doped GaAs power MESFET. The structure consists of a 1 μm thick undoped buffer layer, a thin active layer doped with mid $10^{17}/\text{cm}^3$ (high-doped layer), a thick active layer doped with mid $10^{16}/\text{cm}^3$ (low-doped layer), and an undoped GaAs layer for surface passivation.

doped with mid $10^{16}/\text{cm}^3$ (low-doped layer), and an undoped GaAs layer for surface passivation. The thickness of the low-doped layer was designed to be twice as thick as the depletion layer width after gate formation. The role of this layer is to decrease the gate capacitance and to improve the Schottky characteristics of the gate. The high-doped layer acts as a main channel for carriers and provides an uniform transconductance. Thickness and doping concentration were optimized by DC characteristics such as pinch-off voltage, gate-to-drain breakdown voltage, and transconductance. In order to improve linearity by reducing the output conductance, GaAs/AlGaAs superlattices were introduced into the buffer layer. The layer structure was prepared by molecular-beam-epitaxy on 3 inch semi-insulating GaAs wafer.

MESFET's with a total gate width of 16 mm having 200 μm-wide fingers were fabricated using 3–inch wafer process. In order to obtain a low knee voltage by reducing source resistance, gate-to-source spacing was minimized. Wet etching was used for device isolation, followed by the formation of AuGe/Ni ohmic contacts. The typical value of specific contact resistance was about $2\times10^{-6}\ \Omega\cdot\text{cm}^2$. Ti/Pt/Au gates with a length of 0.8 μm were fabricated using lift-off process. The fabricated MESFET's were protected with a thin layer of Si_3N_4 and the source pads were connected by airbridges. After thinning the wafer to 100 μm, a gold metal was evaporated on the backside to reduce thermal resistance. All devices were finally passivated using 0.8 μm-thick Si_3N_4 film to enhance reliability.

Fig. 2 shows the DC transfer characteristic of 16 mm-width power MESFET, which shows uniform transconductance for the gate voltage in the range from -2.0 V to $+0.5$ V. We obtained the drain saturation current (I_{dss}) of 4.05 A and the gate-to-drain breakdown voltage (BV_{gd}) of 28 V at a gate current density of 1 mA/mm. The current cutoff frequency (f_t) of 400 μm-wide device (2×200 μm) measured at the bias condition for power operation ($V_{\text{gs}}=-2.1$ V and $V_{\text{ds}}=3.3$ V), was around 18 GHz.

III. Power Amplifier Design and Fabrication

For the design of matching circuits, load and source impedances for both the output power and PAE were measured for the first stage and the second stage MESFET by the load-pull

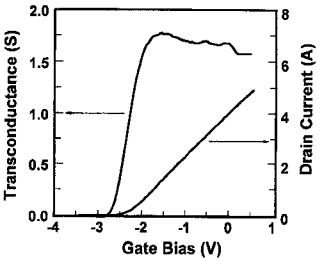
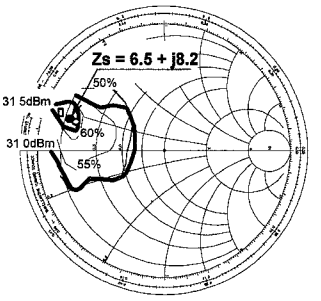
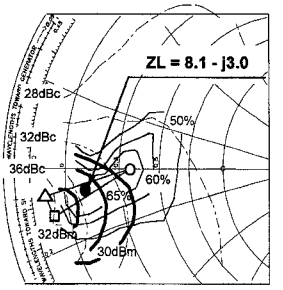


Fig. 2. Gate transfer characteristic of 16 mm-width power MESFET, which shows uniform transconductance over all operating gate bias.



(a)



(b)

Fig. 3. The contours of output power, PAE, and IM3 of the 2nd stage MESFET (———: output power, ———:PAE, —·—: IM3 at an output power of 26 dBm, □: maximum output power, ○: maximum PAE, △: minimum IM3). (a) Source-pull contours. The optimum source(Z_s) was determined by the trade off between the maximum output power and the maximum PAE. (b) Load-pull contours. The optimum load (Z_L)was determined by considering the maximum output power, the maximum, and the minimum IM3.

method using an input and an output tuner. Fig. 3 shows the contours of output power, PAE, and the IM3 at an output power of 26 dBm for the second stage MESFET. We determined optimum source impedance of $6.5+j8.2\ \Omega$ occurred between the maximum output power and the maximum PAE impedances, and the optimum load impedance of $8.1-j3.0\ \Omega$ considering the maximum output power (32.1 dBm), the maximum PAE (68%), and the minimum IM3 (-37 dBc). An output power of 31.7 dBm, a PAE of 66%, and IM3 of -33 dBc were achieved at the optimum impedances. Fig. 4 shows the third order product and the fundamental output power as a function of input power at the optimum impedances using the two-tone test. The 2nd and 3rd harmonics of the 2nd MESFET at an input power of 20 dBm were measured to be -45 dBc and -35 dBc, respectively. These characteristics of the newly developed power MESFET satisfied the requirements for low distortion.

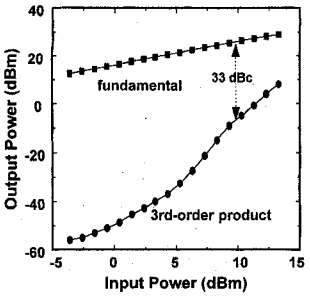


Fig. 4. The third-order product and the fundamental output power of the 2nd stage MESFET as a function of input power.

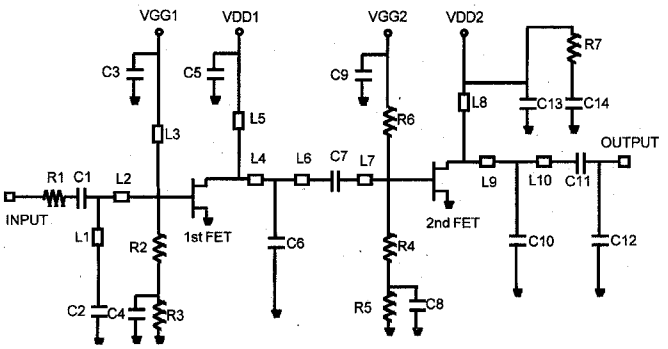


Fig. 5. Circuit diagram of the power amplifier for dual-mode cellular phones. This structure shows low impedances at the drain terminal port for the 2nd and the 3rd harmonic frequencies.

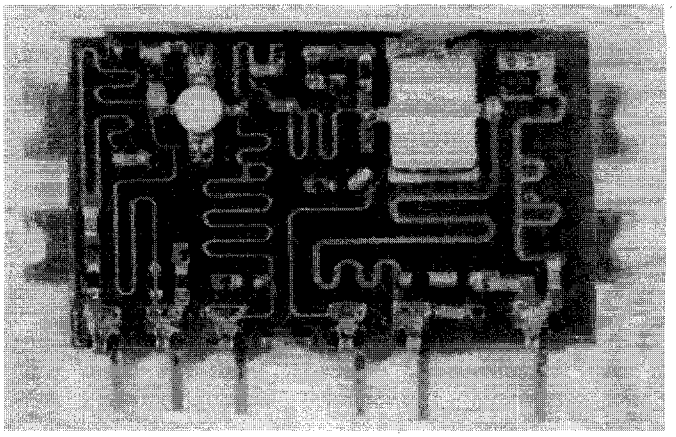


Fig. 6. Top view photograph of the dual-mode power amplifier with a size of 11.9 × 21.0 mm^2.

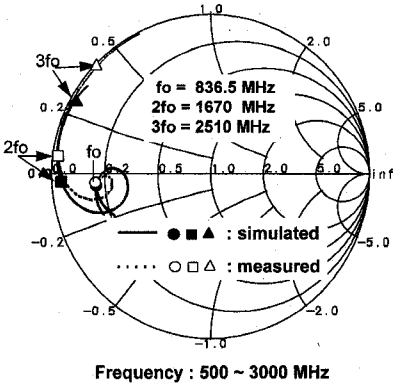


Fig. 7. The simulated and measured impedance contours of an output circuit at the drain terminal of 2nd MESFET as a function of frequency. Solid line shows the simulation result; dashed line shows the measured result.

The circuit diagram of the power amplifier for the dual-mode cellular phone is shown in Fig. 5. It consists of two stages to obtain a small-signal gain of more than 31 dB. The total gate width of the first stage MESFET and the second stage MESFET are 3.2 mm and 16 mm, respectively. One of the important issues in designing an amplifier for dual-mode applications is the selection of a bias point. From the results of the two-tone tests for the 2nd stage MESFET, the bias circuits were designed for class AB (I_{ds} = 400 mA ~ 10% I_{dss}) operation. The gate bias of −3 V is supplied through divider resistors with a predetermined voltage. Resistive matching circuits were employed in both input matching circuit and gate bias circuits for more stable operation. The matching networks were conjugately matched to an optimum load and an optimum source impedance using a linear simulator.

Fig. 6 shows a top view photograph of the dual-mode power amplifier with a size of 11.9 × 21.0mm^2. The matching and bias circuits are composed of microstrip transmission lines, chip capacitors and resistors (1005-type). Glass-based epoxy (FR-4) is used as the substrate, and total cost of the power amplifier can be reduced. Although this low cost substrate has a high loss tangent of 0.018, high power performance was achieved for both AMPS and CDMA modes, simultaneously.

In the design of the 2nd stage amplifier, an output matching circuit was designed to have low impedances for the frequencies corresponding to the 2nd and the 3rd harmonics in order to reduce the harmonics. Conventionally, the output matching circuits at the drain port are typically terminated by a short circuit for the 2nd harmonic frequency and by an open circuit for the 3rd harmonic frequency. In this work, we focused on designing the output circuit for the 2nd and the 3rd harmonic frequencies to provide a short circuit to reduce both the harmonics and the circuit losses. The length of the drain bias line with a width of 300 μm was designed to be shorter than quaterwavelength.

On-printed circuit board (PCB), in-circuit probing measurements of the matching circuits of the amplifier were performed in order to tune the matching circuits designed by a linear simulator. PCB patterns of matching circuits were prepared by varying the length of microstrip lines and the capacitance of chip capacitors with ±10% variations from the simulated value. The patterns with ground-signal-ground (GSG) pads were measured using 1250 μm wide-pitch probes to obtain a match with the simulated results. Advantages of this method compared with that using a test fixture were to lower the fabrication cost and to directly tune the circuits on-PCB with a simple calibration by understanding the behavior of impedance matching. Fig. 7 shows the simulated and the measured impedance contours of the output matching circuit at the drain terminal of the 2nd MESFET as a function of frequency. At the fundamental frequency of 836.5 MHz, the measured impedance was well matched to the simulated one.

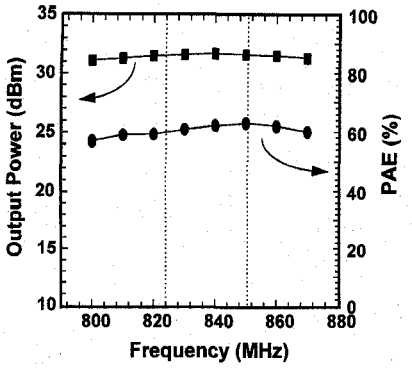


Fig. 8. Output power and PAE characteristics measured at a 3.3 V, Pin = 7 dBm as a function of frequency. At the frequency range between 824 MHz and 849 MHz, the output of 31.5 dBm ±0.2 dB and the minimum PAE of 60% are achieved.

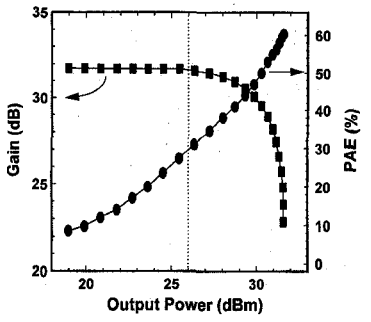


Fig. 9. Gain and PAE characteristics of the power amplifier as a function of output power at 836.5 MHz. At the output power level lower than 26 dBm, the power gain of 31.5 dB is maintained within ±0.4 dB deviation.

IV. Performance of Amplifier

Fig. 8 shows the output power and PAE of the power amplifier. It was measured at a supply voltage of 3.3 V and an input power of 7 dBm as a function of frequency. At the frequency range between 824 MHz and 849 MHz, the output power of 31.5 dBm is maintained within ±0.2 dBm, and the minimum PAE of 60% is obtained. These are higher than the requirements for AMPS mode. Fig. 9 shows the gain and PAE of the power amplifier as a function of output power at 836.5 MHz. For output powers lower than 26 dBm, the power gain of 31.5 dB is maintained within ±0.4 dB deviation. The PAE for AMPS at the output power of 31.5 dBm and that for CDMA at 26 dBm were measured to be 61% and 30%, respectively. The fundamental output power and the harmonics as a function of input power with a fundamental frequency of 836.5 MHz are shown in Fig. 10. The 2nd and the 3rd harmonics of the amplifier at an output power of 31.5 dBm were measured to be −50 dBc and −51 dBc, respectively, which are much lower than those previously reported [5], and are lower than those measured at the 2nd stage MESFET. From these results, the method used for the design of the output matching circuits was effective in reducing the harmonics. The intermodulation distortion of the amplifier versus input power was measured using two-tone frequencies, 836.5000 and 836.9425 MHz. The IM3 and the IM5 at an output power of 26 dBm, as shown in Fig. 11, were measured to be −32 dBc and −45 dBc, respectively, which are suitable for CDMA mode applications.

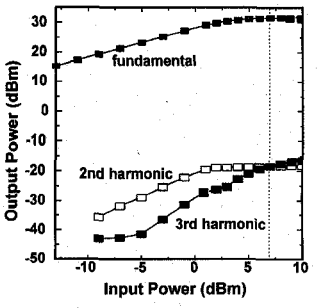


Fig. 10. The 2nd and 3rd harmonic characteristics as a function of input power with fundamental frequency of 836. MHz. The 2nd and 3rd harmonics of the amplifier at an output power of 31.5 dBm are −50 dBc and −51 dBc, respectively.

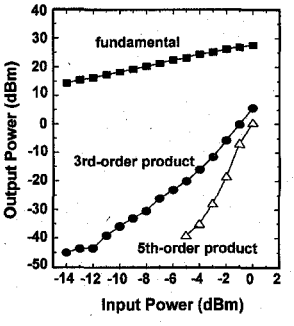


Fig. 11. The intermodulation distortion of the amplifier with the input power was measured using two-tone frequencies, 836.5000 and 836.9425 MHz. The IM3 and the IM5 at an output power of 26 dBm are −32 dBc and −45 dBc, respectively.

The measured characteristics of the dual-mode power amplifier are summarized in Table I.

High power, high efficiency, and low distortions for the dual-mode applications were achieved by determining the optimum impedances in the circuit design in consideration of the maximum output power, the maximum PAE, and the minimum IM3 using the load-pull method. The performance of power amplifier developed in this work is better than the previous results with an output power of over 31.1 dBm and a PAE of 60% at 3.5 V [5] for analog phones. Although the measured phases of the 2nd and the 3rd harmonic frequencies in Fig. 7 were deviated from the simulated ones to some degree, the power amplifier shows low harmonics and good linearity. This performance is attributed to high reflection of the output matching circuit for the harmonic frequencies and to the linear power MESFET.

V. Conclusion

A power amplifier operating at 3.3 V has been developed for CDMA/AMPS dual-mode cellular phones. It consists of linear GaAs power MESFET's and an output matching circuit which reduces the 2nd and the 3rd harmonics. For the circuit design, the optimum load and source impedances of the MESFET were determined by the tradeoff between the power performance and the linearity using the load-pull method. For AMPS mode, the fabricated amplifier shows an output power of 31.5 dBm and a power-added efficiency of 61%. For CDMA mode, the third-order intermodulation distortion of −32 dBc, the fifth-order

TABLE I
SUMMARY OF THE MEASURED CHARACTERISTICS OF DUAL-MODE POWER AMPLIFIER. FOR AMPS MODE, OUTPUT POWER OF 31.5 dBm AND PAE OF 61% WERE ACHIEVED. FOR CDMA MODE, THE IM3 OF −32 dBc AND THE IM5 OF −45 dBc WERE ACHIEVED AT AN OUTPUT POWER OF 26 dBm

Common Specifications	
Frequency Range	824~849MHz
Amplifier Size (PCB)	11.9 x 21.0 mm^2
Small Signal Gain	31.5 dB
Supply Voltage	3.3V
AMPS Mode @ 836.5 MHz, Pin=7dBm	
Output Power	31.5 dBm
Power-Added Efficiency	61%
Harmonics (2fo)	-50 dBc
Harmonics (3fo)	-51 dBc
CDMA Mode @ 836.5 MHz, Pout=26 dBm	
Gain Linearity (≤26dBm)	< ± 0.4 dB
Power-Added Efficiency	30%
Intermodulation (3rd)	-32 dBc
(5th)	-45 dBc

intermodulation distortion of −45 dBc and a power-added efficiency of 30% were obtained at an output power of 26 dBm. The most significant result is the simultaneous achievement of high power, high efficiency, and low distortions. These results are attributed to linear power MESFET's and the 2nd and the 3rd harmonic termination in the output matching circuit. Finally, the power amplifier developed in this work is expected to be used for CDMA/AMPS dual-mode cellular phones in near future.

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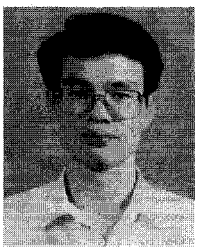


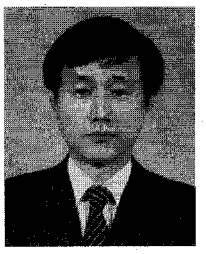
Sung-Jae Maeng was born in Chungnam, Korea on May 2, 1960. He received the B.S. degree in inorganic materials science engineering in 1984 from Seoul National University and the M.S. degree in materials and science engineering in 1986 from Korea Advanced Institute of Science and Technology (KAIST).

After the M.S. degree he joined Electronics and Telecommunications Research Institute (ETRI) to work on GaAs MESFET technology. He is presently a Senior Member of the engineering staff in ETRI's semiconductor technology division. He is currently working toward the Ph.D. degree at KAIST. He is involved with the development of GaAs power amplifier and GaAs MMIC design. His research interests are in the area of modeling and designing microwave materials, devices, and circuits.

Soung-Soon Chun was born in Seoul, Korea on August 13, 1935. He received the B.S. degree in mining engineering from Hanyang University in 1958. He received the M.S. degree in mechanical engineering from University of Marquette in 1964 and Ph.D. degree in metallurgical engineering from Stevens Institute of Technology in 1968.

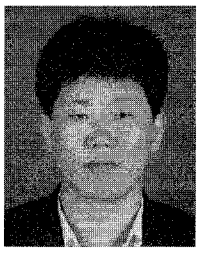
From 1968 to 1972, he was an Assistant Professor at University of Utah. He joined the faculty of Korea Advanced Institute of Science and Technology, in 1972, where he is presently Professor of Electronic Materials Science and Engineering. He is the author/coauthor of over 130 research papers in the area of electronic materials.

Dr. Chun is a member of AIME and ASM.



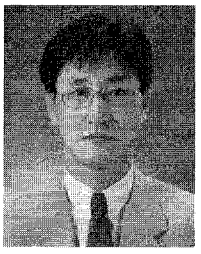
Jong-Lam Lee was born in Seoul, Korea, on April 6, 1958. He received the B.E. degree in metallurgical engineering from Hanyang University in 1980, and M.S. and Ph.D. degrees in materials science and engineering from Korea Advanced Institute of Science and Technology in 1982 and 1985, respectively. From June 1985 to Oct. 1986 he joined Northwestern University and Michigan Technological University as a Postdoctoral Fellow.

He joined Electronics and Telecommunications Research Institute (ETRI) in 1986 as a Senior Researcher. From 1987 to 1988, he was involved in the fabrication of MESFET's and HEMT's. From 1989 to 1990, he worked on the growth of AlGaAs and GaAs by molecular beam epitaxy and investigated surface passivation of compound semiconductor using $(NH_4)_2S_x$ and their characterization using slow positron beam technique at the University of Tsukuba in Japan, as a Research Associate. From 1991 to 1994, he worked on development of low-voltage-operation GaAs power MESFET for mobile communications and transferred the fabrication technology to industry for commercial production. He is now the Head of Microwave Circuits Section of ETRI. His research covers compound semiconductor process including surface passivation and metal/semiconductor contacts, basics of defects in semiconductor materials and understand of their roles on electrical characteristics, and microwave and milimeter wave devices.



Chang-Seok Lee was born in Seoul, Korea on March 29, 1961. He received the B.S. degree in electronic engineering from the Kyung-buk National University and the M.S. degree from Korea Advanced Institute of Science and Technology (KAIST) in 1984 and 1986, respectively.

In 1986, he joined Electronics and Telecommunications Research Institute (ETRI) at Taejon, Korea. Since joining ETRI in 1986, he has been involved in the development of GaAs digital/analog IC's. His research interest is high yield MMIC design.



Kwang-Jun Youn was born in Cheon An, Korea on February 4, 1962. He received the B.S. degree in electronic engineering from the Chung-Nam National University and the M.S. degree from the Yonsei University, Korea in 1985 and 1987, respectively.

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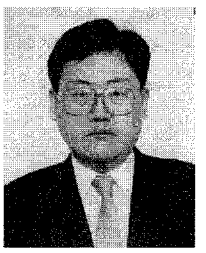

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